SGS-THOMSON MICROELECTRONICS

# 486 COMMON SOCKET IMPLEMENTATION

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## 1. Overview

This document provides detailed information regarding the differences in pinouts between SGS-THOMSON Microelectronics(ST) and Intel 486 PGA devices and specifies electrical connections that allow a single motherboard design to support all of the listed devices. This implementation is intended to be a guideline to eliminate conflicts due to pinout differences only.

This common socket specification is intended to support the following devices:

SGS-THOMSON ST486 DX2
CYRIX Cx486 DX2
SGS-THOMSON ST486 DX2V
SGS-THOMSON ST486 DX4V
SGS-THOMSON ST5x86
CYRIX Cx5x86
INTEL i486 DX2 SL & WB Enhanced
INTEL i486 DX4
AMD AM486 DX2 (Future SL & WB Enhanced)
AMD AM486 DX4 (Future SL & WB Enhanced)

For additional information, please contact SGS-Thomson Microelectronics. Information in this document is subject to change without notification. The following documents were used as references: Intel486 Microprocessor Family, AM486 Microprocessor Family System Design Consideration. Any functions not disclosed in the referenced documents are NOT covered by the scope of this specification.

## 2. CPU Features

Each of the CPUs supported in this common socket specification is 486 bus compatible yet has a unique set of features that impacts the device pinout. Table 2-1 lists the differences in the CPU feature sets.

**Table 2-1. CPU Enhanced Features**

| CPU | VOLTAGE | WRITE-BACK | SMM & POWER MANAGEMENT | CORE CLOCK CONTROL | JTAG |
|---|---|---|---|---|---|
| ST486DX2<br>Cx486DX2 | 5 V | yes | yes | no | no |
| ST486DX2V<br>Future AM486DX2 | 3.45V, 5V I/O | yes | yes | no | no |
| ST486DX4V<br>Future AM486DX2 | 3.45V, 5V I/O | yes | yes | 2x, 3x | no |
| ST5x86<br>Cx5x86 | 3.45V, 5V I/O | yes | yes | 0.5x, 1x, 2x, 3x | yes |
| Intel i486DX/DX2 SL & WB Enh. | 5 V | yes | yes | no | yes |
| IntelDX4 | 3.3 V, 5 V I/O | no | yes | 2x, 2.5x, 3x | yes |

## 3. Pin Differences

Table 3-1 lists those pins with signal assignments that are not consistent for all of the CPUs. Table 3-1 also specifies the appropriate connections for a common socket implementation. All the pins that are not listed have identical signal assignments for all CPUs shown in the table. Therefore when implementing a common socket, all pins not listed should have identical connections to the system logic regardless of the CPU type.

**Table 3-1. CPU Pin Assignment**

| PIN NUMBER | SIGNAL NAME | | | | | | Note |
|---|---|---|---|---|---|---|---|
| | ST486DX2 Cx486DX2 | ST486DX4V ST486DX2V | ST5x86 Cx5x86 | Future AM486DX2 AM486DX4 | i486DX/DX2 SL & WB Enhanced | IntelDX4 | |
| A3 | NC | NC | TCK | | TCK | TCK | 1 |
| A10 | SUSPA# | INVAL | INV | INV | INV | NC | |
| A12 | SMI# | HITM# | HITM# | HITM# | HITM# | NC | |
| A13 | RPLSET1 | SUSPA# | SUSPA# | NC | NC | NC | |
| A14 | NC | NC | TDI | | TDI | TDI | 1 |
| B10 | NC | SMI# | SMI# | SMI# | SMI# | SMI# | 2 |
| B12 | TEST | RPLSET1 | CACHE# | CACHE# | CACHE# | NC | |
| B13 | WM_RST | RPVAL# | NC | WB/WT# | WB/WT# | NC | |
| B14 | NC | RPLSET0 | TMS | TMS | TMS | TMS | 1 |
| B16 | NC | NC | TDO | | TDO | TDO | 1 |
| C10 | SMADS# | WM_RST | WM_RST | SRESET | SRESET | SRESET | 3 |
| C12 | RPLSET0 | SMADS# | SMADS# | SMIACT# | SMIACT# | SMIACT# | 2, 4 |
| C13 | RPVAL# | TEST | NC | | NC | NC | |
| G15 | SUSP# | SUSP# | SUSP# | STPCLK# | STPCLK# | STPCLK# | 5 |
| J1 | NC | NC | NC | NC | VCC | VCC5 | 6 |
| R17 | HITM# | CLKMUL | CLKMUL | CLKMUL | NC | CLKMUL | 7, 8 |
| S4 | INVAL | VOLDET | VOLDET | VOLDET | NC | VOLDET | |

**Notes**

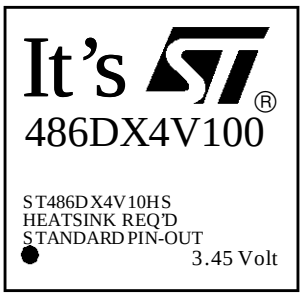
1) TCK, TDI, TMS, TDO are JTAG pins.
2) SMI# and SMADS# may be programmed to be SL compatible as SMI# and SMIACT# from rev 4.0.
3) SRESET and WM_RST have the same function.
4) SMIACT# and SMADS# have the same function.
5) STPCLK# and SUSP# have the same function.
6) J1 is NC on the ST 3.45 Volt CPUs.
7) The 2.5 ratio is supported only by the Intel DX4.
8) The CLKMUL must be grounded externally in the ST486DX2V and the AM486DX2.

**4. Device Marking**

The SGS-THOMSON devices have two kinds of pinout: the old pinout and the standard pinout. The old pinout was defined prior to the introduction of the Intel SL-Enhanced and WB-Enhanced CPUs. The pins concerning the enhanced features do not have the same location as in the latest Intel socket. In the standard pinout these pins have been placed in accordance with the Intel socket. The old pinout concerns the ST486DX2 5 Volt whatever the clock frequency is. Figure 4-1 shows the marking of these devices.

**Figure 4-1. Old Pinout Markings**


**Figure 4-2. Standard Pinout Marking**




The standard pinout concerns the ST486DX4 devices and the 3 Volt devices. On these devices a special marking "STANDARD PINOUT" has been added. Figure 4-2 shows the marking of these devices.

All the 5 Volt ST486DX2 are manufactured with the old pinout.

All the 3 Volt ST486DX2V and all the ST486DX4V are manufactured with the standard pinout.

Figure 4-3 shows a common socket implementation supporting all the CPUs listed in table 2-1 except the ST486DX2 5 VOLT and the Cx486DX2. This is the recommended design implementation. J1 connection must be: 1-2 for the DX2 parts, 2-3 for the other parts.

A schematic for the common socket connections supporting all the listed 486 CPUs is shown in Figure 4-4. The corresponding jumper settings are listed in Table 4-2.

**Figure 4-3. Simplified Common Socket Schematic**

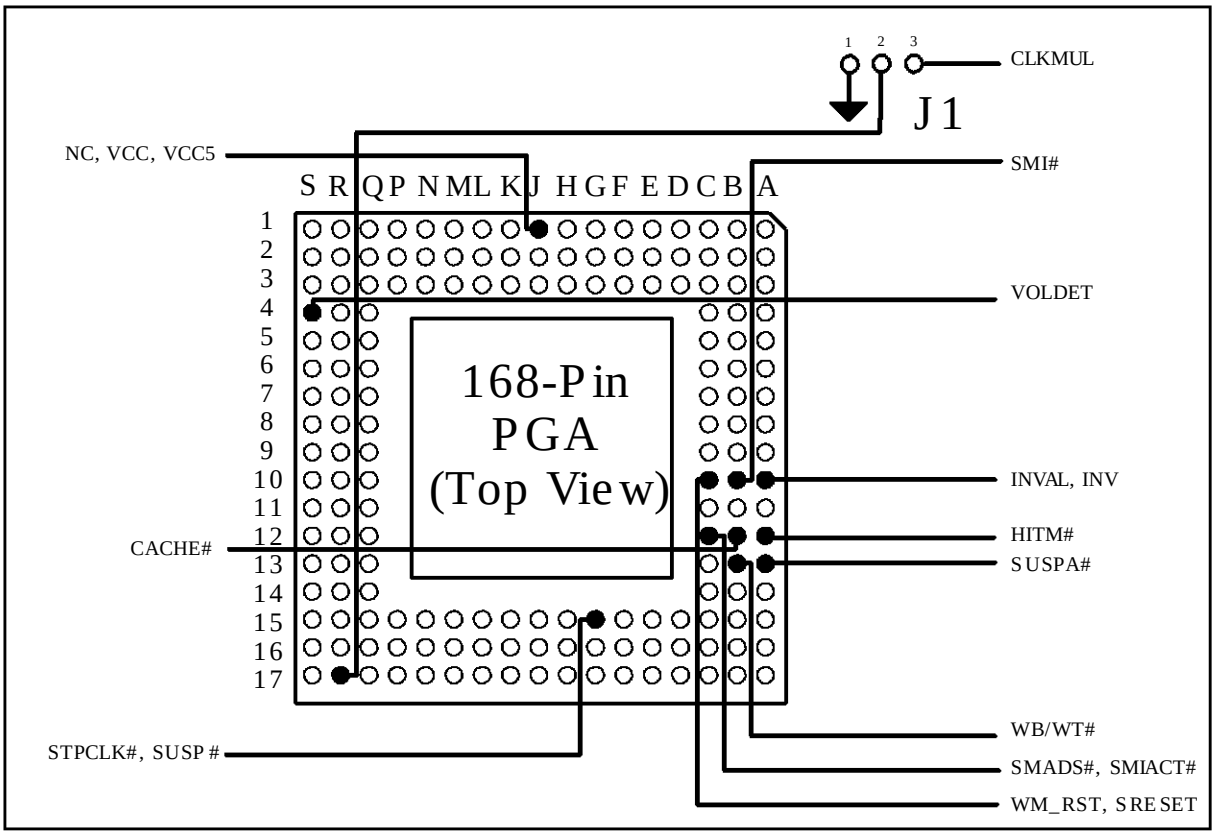


**Figure 4-4. Common Socket Schematic**

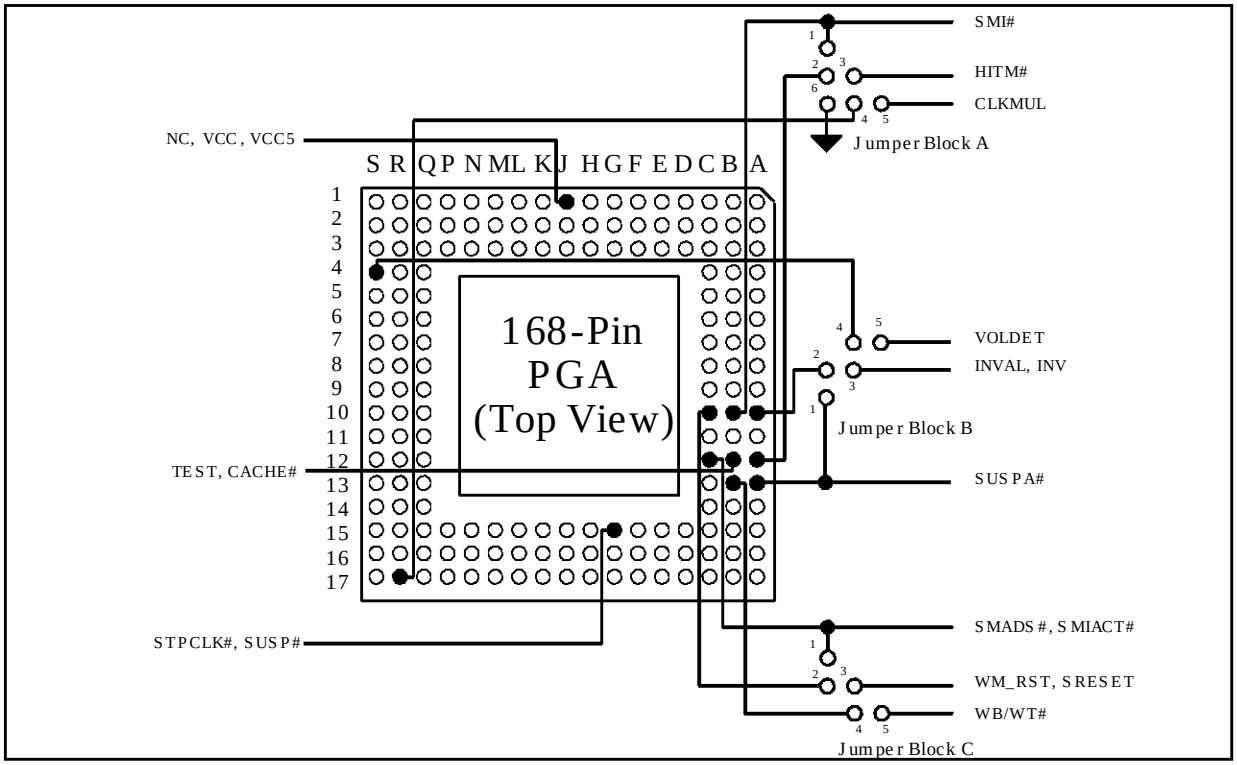



**Table 4-2. Jumper Settings**

| CPU | JUMPER BLOCK A | JUMPER BLOCK B | JUMPER BLOCK C |
|---|---|---|---|
| ST486DX2, Cx486DX2 | 1-2 and 3-4 | | |
| ST486DX2V, Future AM486DX2 WB Enh. | 2-3 and 4-6 | 2-3 and 4-5 | 2-3 and 4-5 |
| ST486DX4V, ST5x86, Cx5x86, Intel 486DX/DX2 SL & WB Enh., IntelDX4, Future AM486DX4 WB Enh. | 2-3 and 4-5 | | |

**Important Notes relative to figure 4-3:**

1) We assume in the common socket of figure 4-3 that the following pins are disabled (default after reset): RPVAL, RPLSET0, RPLSET1.

2) This socket does not support the Cx486DX2. For this device, additional jumpers must be added in order to select the appropriate CPU voltage. On certain old parts of this device pin J1 is VCC 5V and must be isolated.

3) This socket accepts the future AMD 3V Writeback Enhanced CPU DX2 and DX4. The pinout of this CPU is identical to the ST486DX2V except the pin SUSPA# (A13) which is not connected. **Like the ST486DX2V the AM486DX2 must have the CLKMUL pin connected to GND externally**.

4) This socket does not support the 2.5x ratio allowed by the IntelDX4 CPU.

5) In the old ST pinout the location of the TEST pin matches to the location of the CACHE# output pin. A particular attention must be payed on this pin in the application board. The TEST pin must have the zero level